Figure 1: Top-level block diagram of the all-digital sampling rate converter when applied to "CD to DAT" conversion.

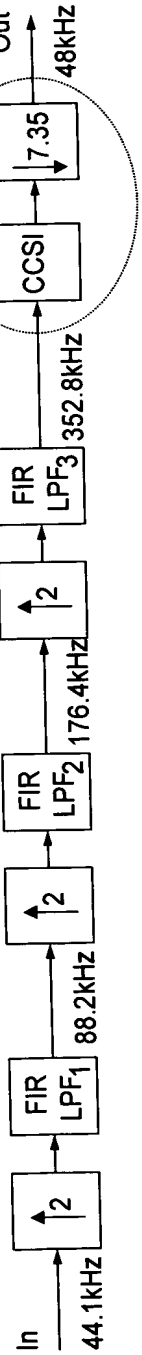


Figure 3: Typical architecture of the sampling rate converter in accordance with the present invention.

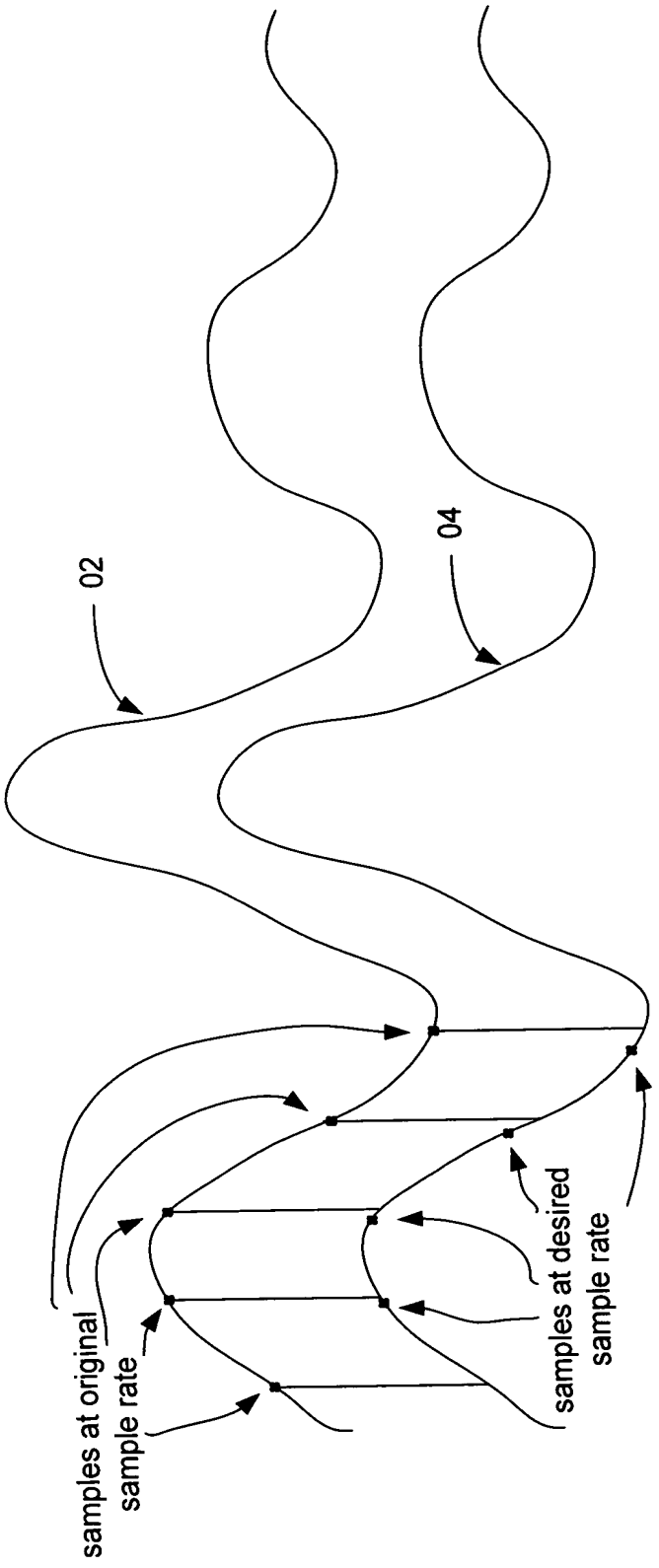


FIG. 2A: Sampling of an example signal

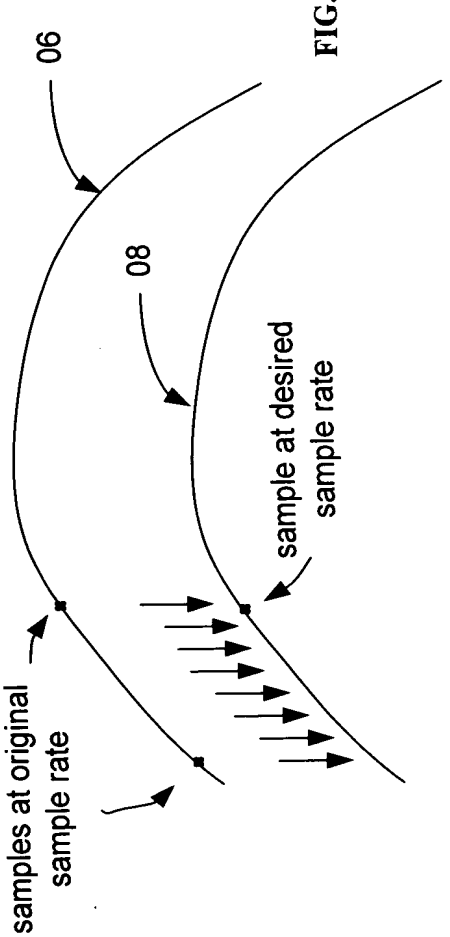


FIG. 2B: Upsampling of an example signal

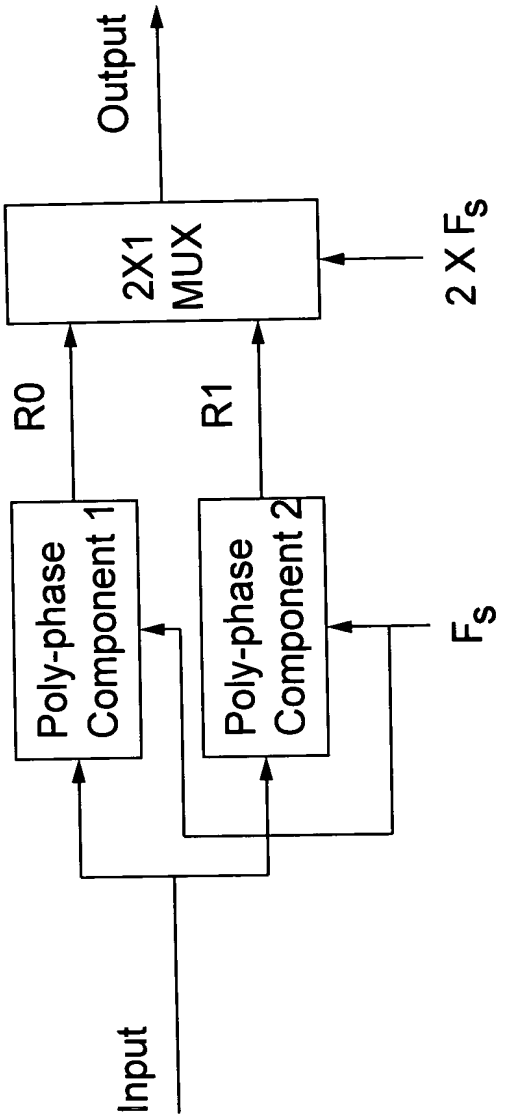


Figure 4: Top level structure of poly-phase implementation of each of the interpolation filters.

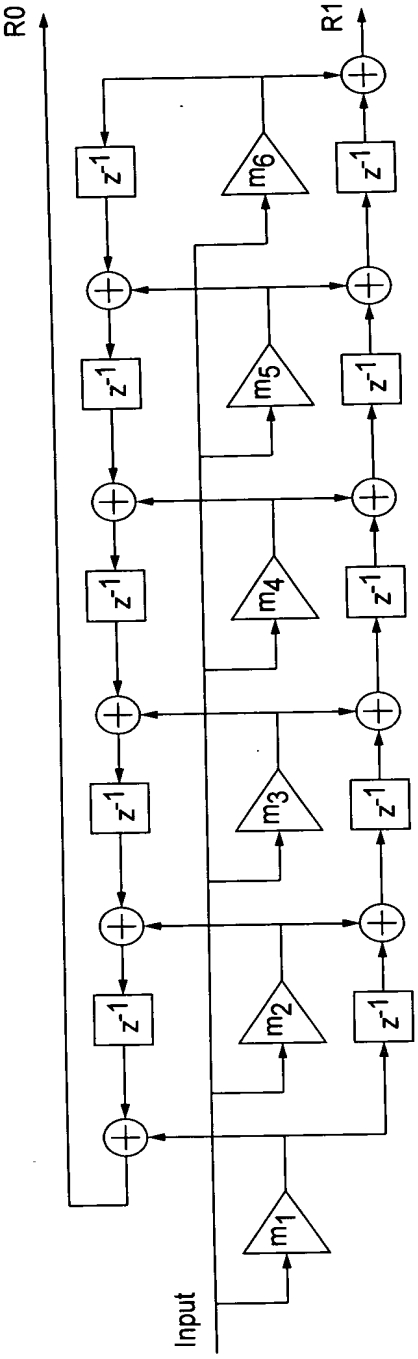


Figure 5: Poly-phase implementation of LPF_3.

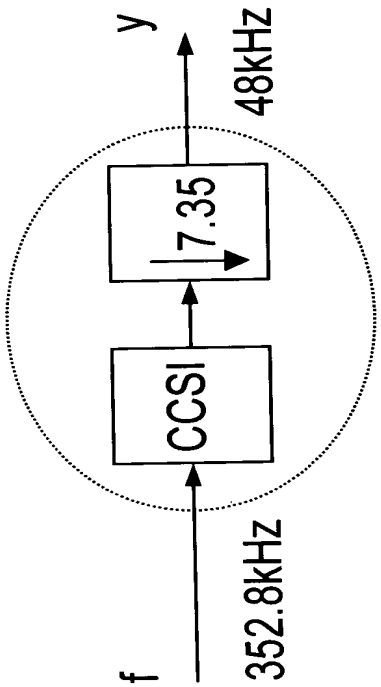


Figure 6: Top level diagram of the Clamped Cubic Spline Interpolator (CCSI) of Figure 3.

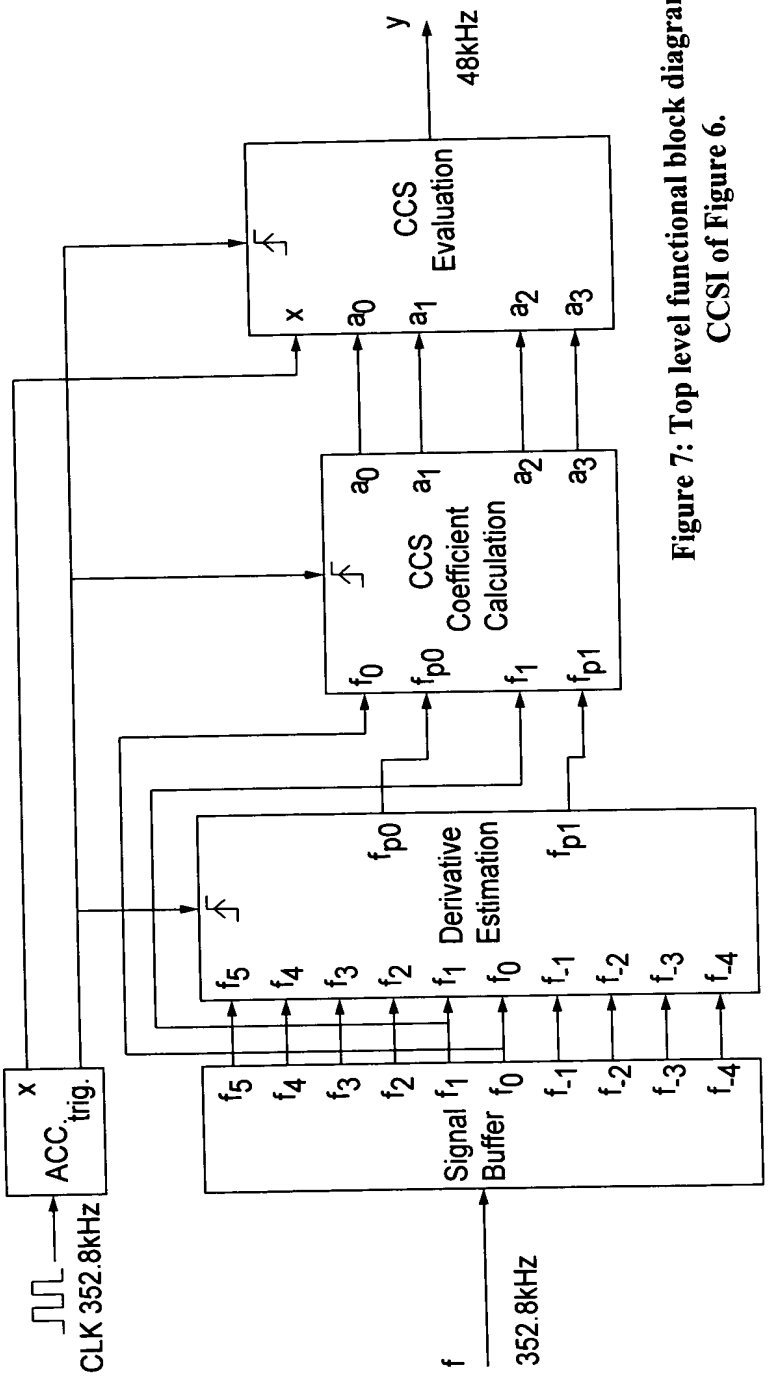


Figure 7: Top level functional block diagram of the CCSI of Figure 6.

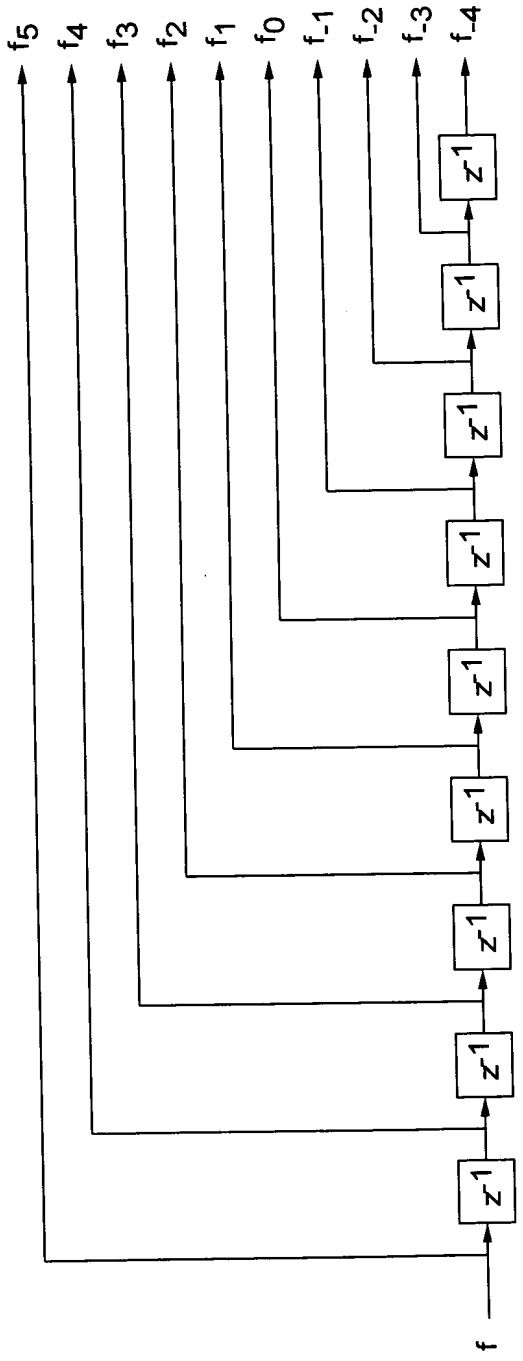


Figure 8: Details of the "Signal Buffer" block of Figure 7.

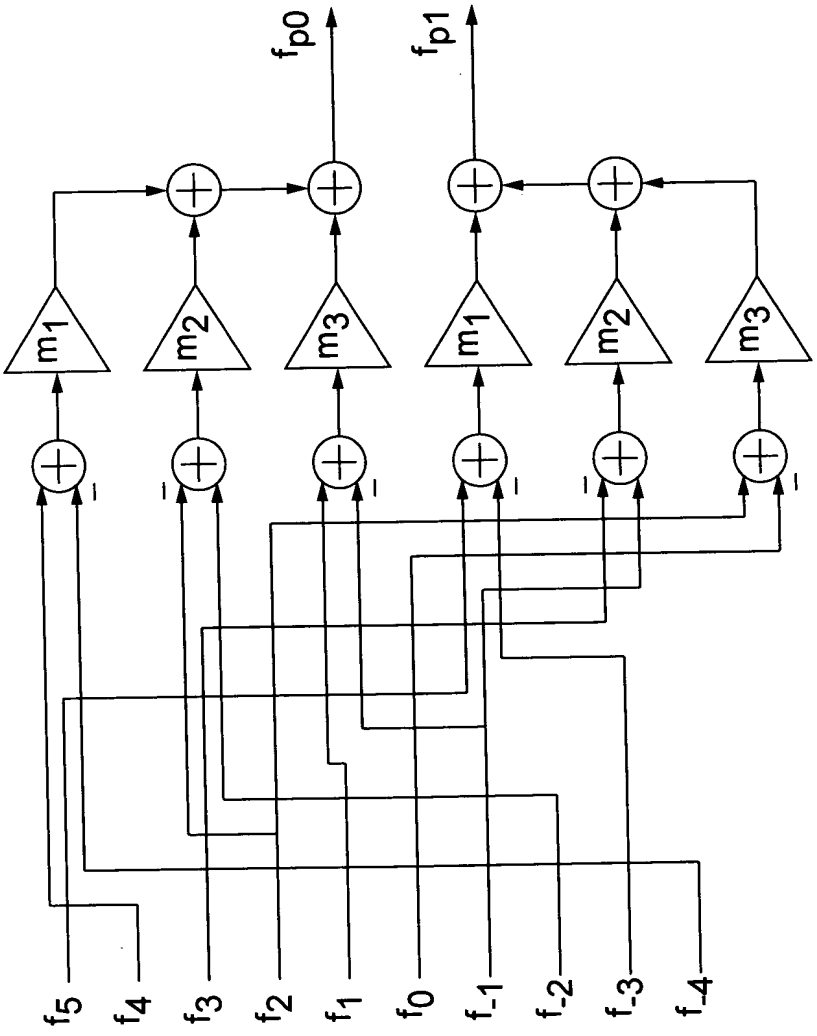


Figure 9: Details of the "Derivative Estimation" block of Figure 7

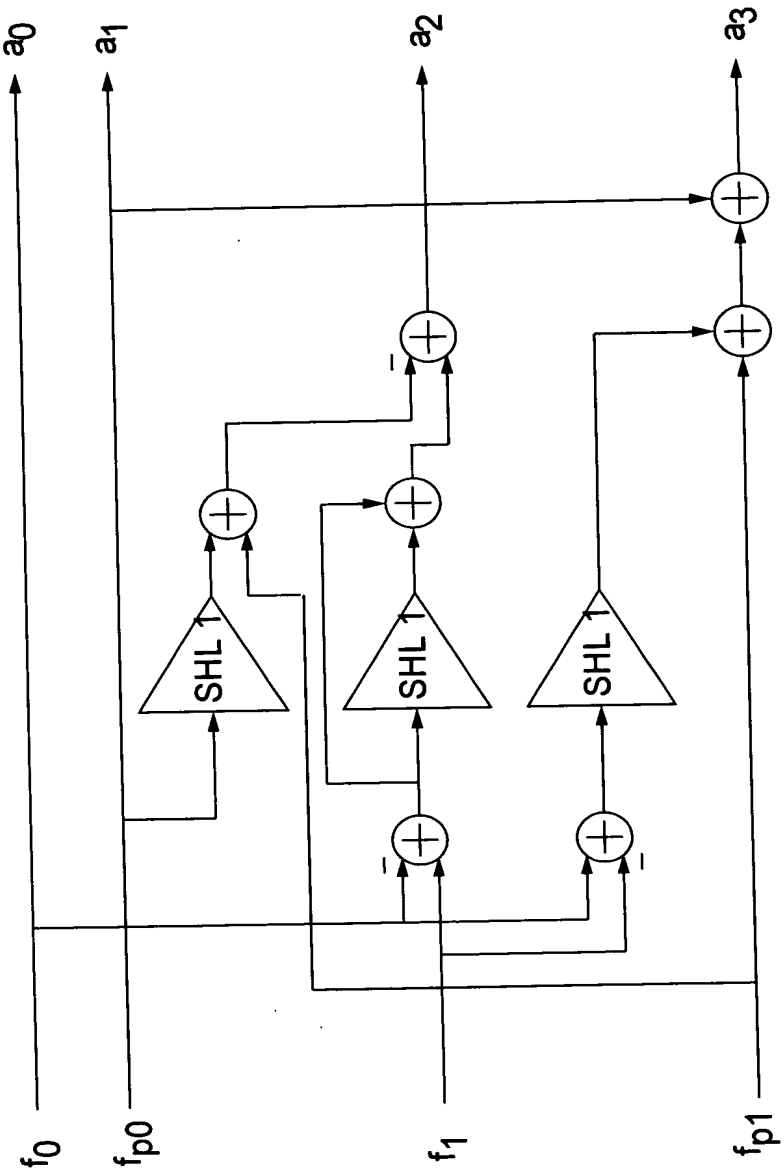


Figure 10: Details of the "CCS Coefficient Calculation" block of Figure 7.

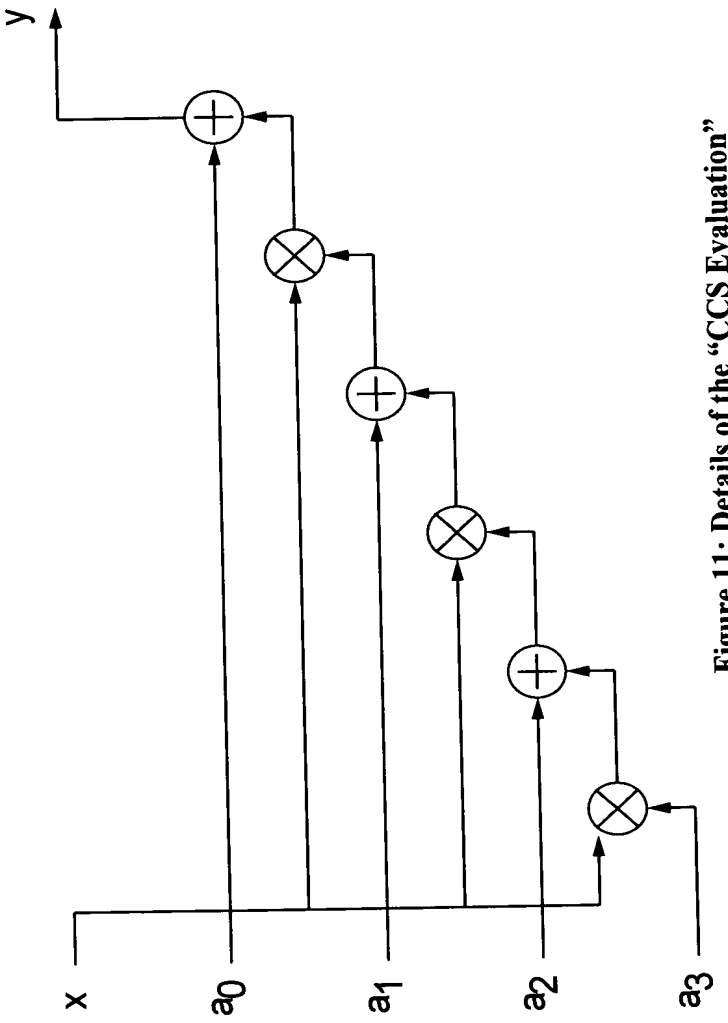


Figure 11: Details of the "CCS Evaluation" block of Figure 7

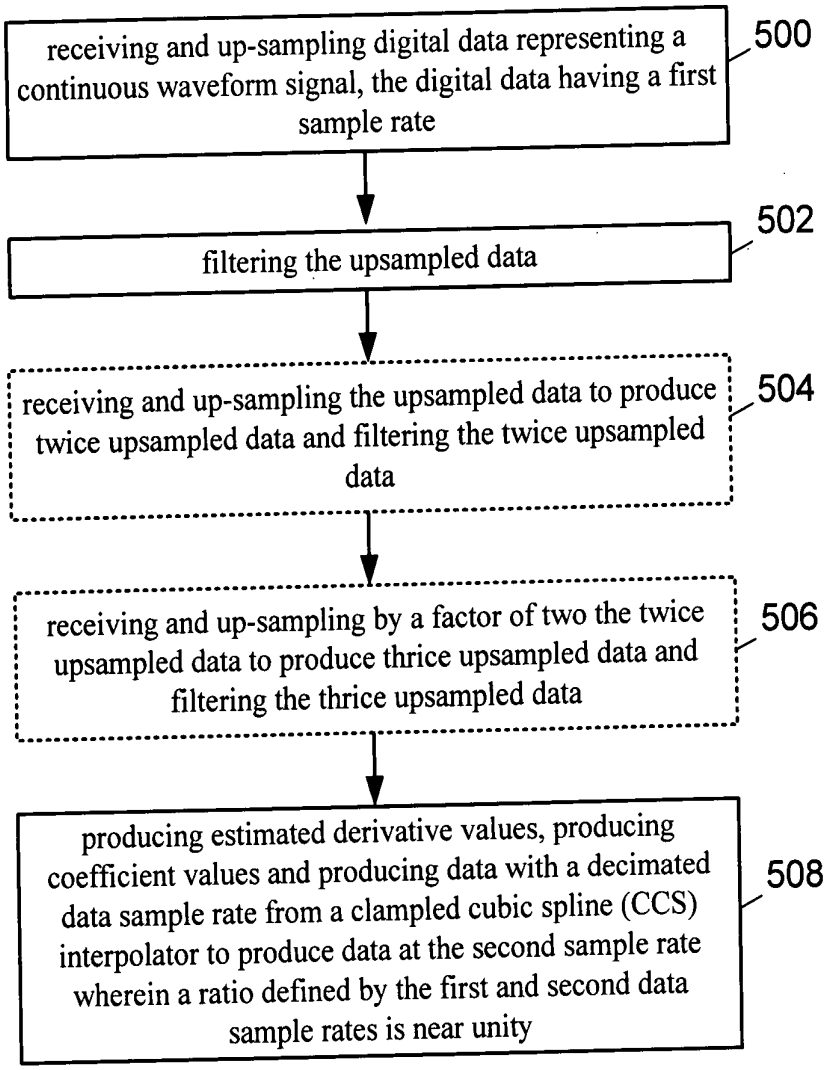


FIG 12A: Method for near unity sample rate conversion

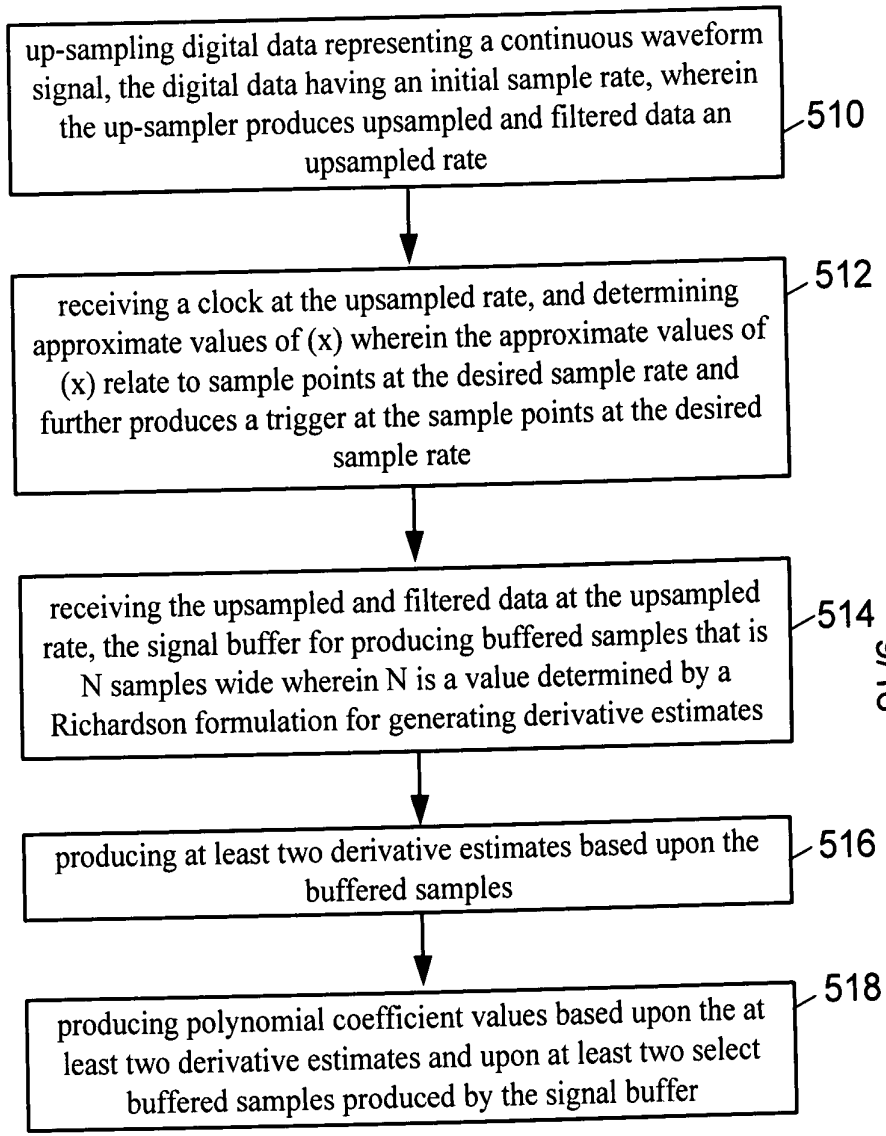


FIG 12B: Method for determining coefficient values as a part of performing near unity sample rate conversion

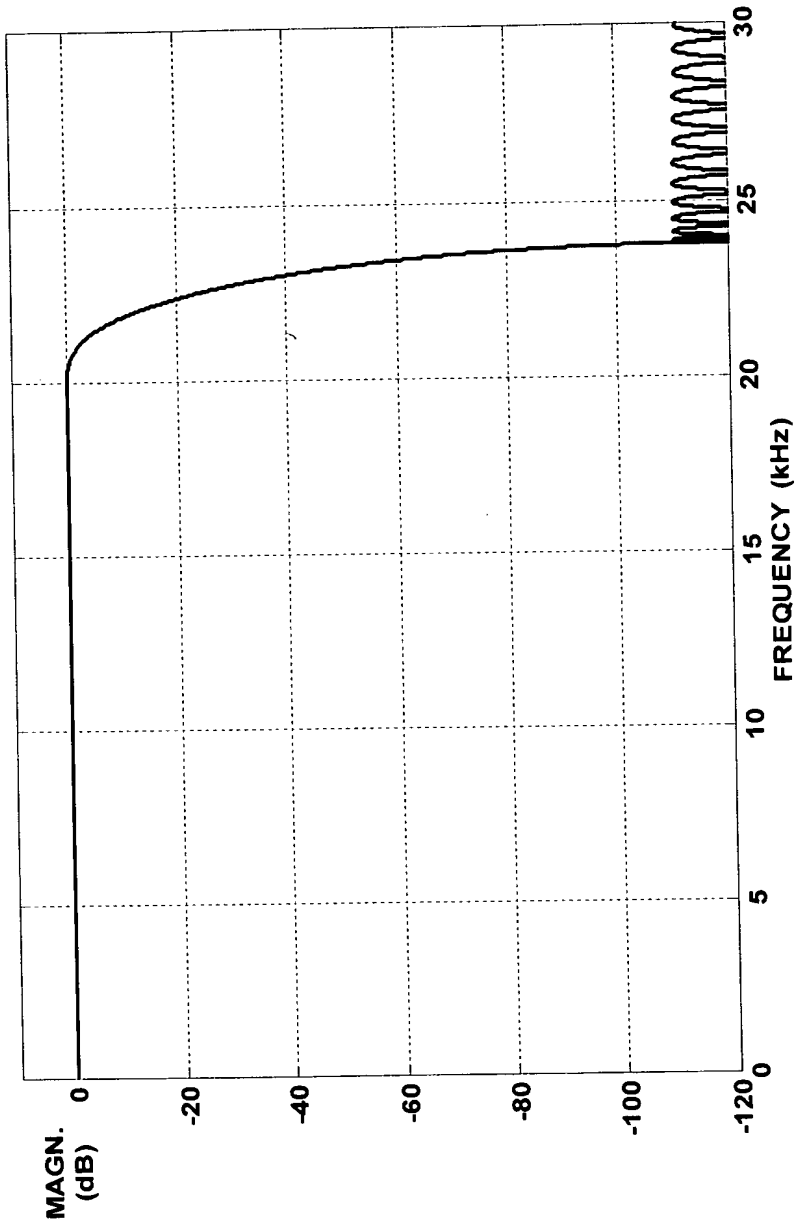


Figure 13: Magnitude response of the CD to DAT converter

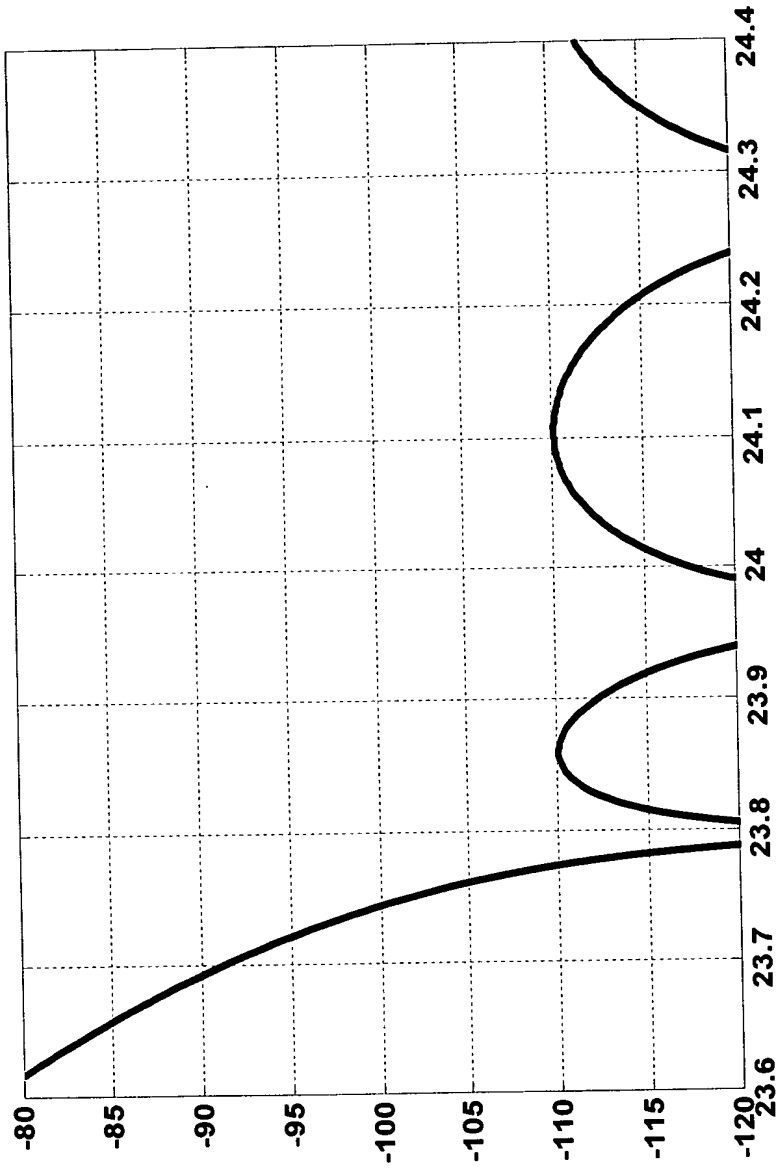


Figure 14: Close-up of the magnitude response shown in Figure 13

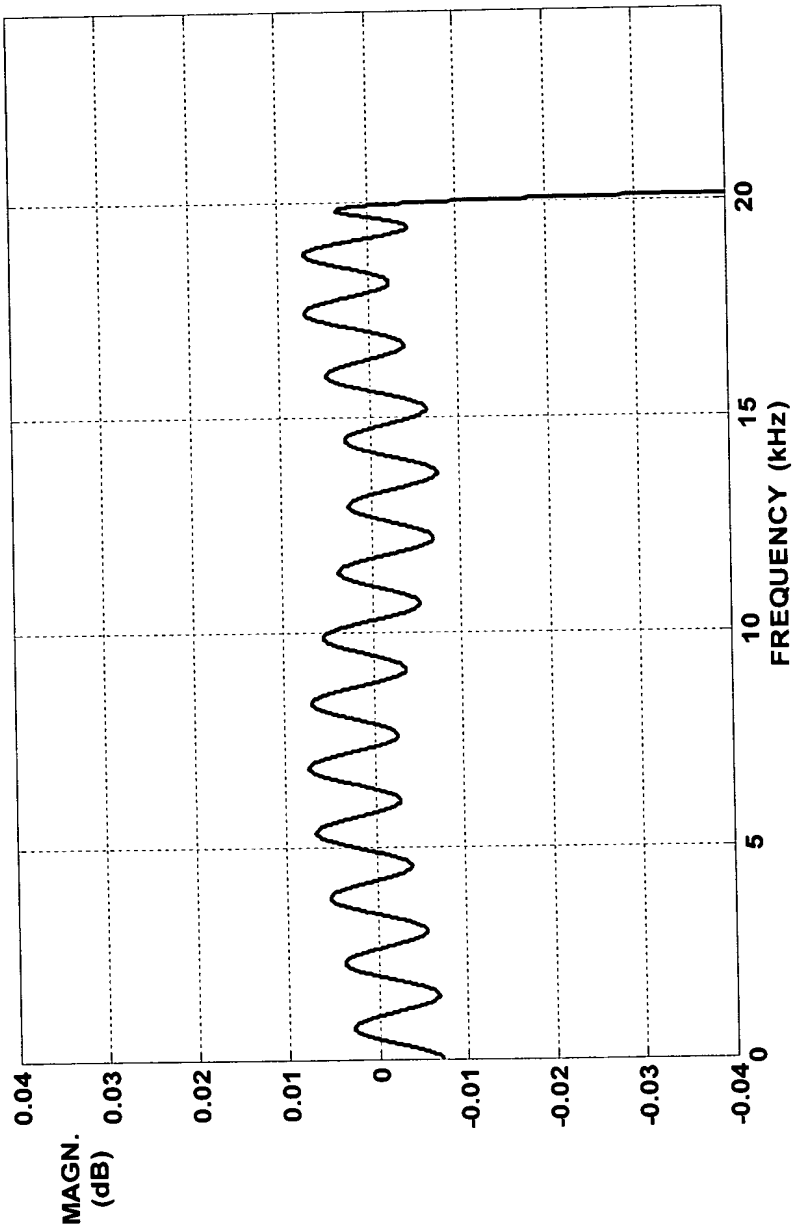
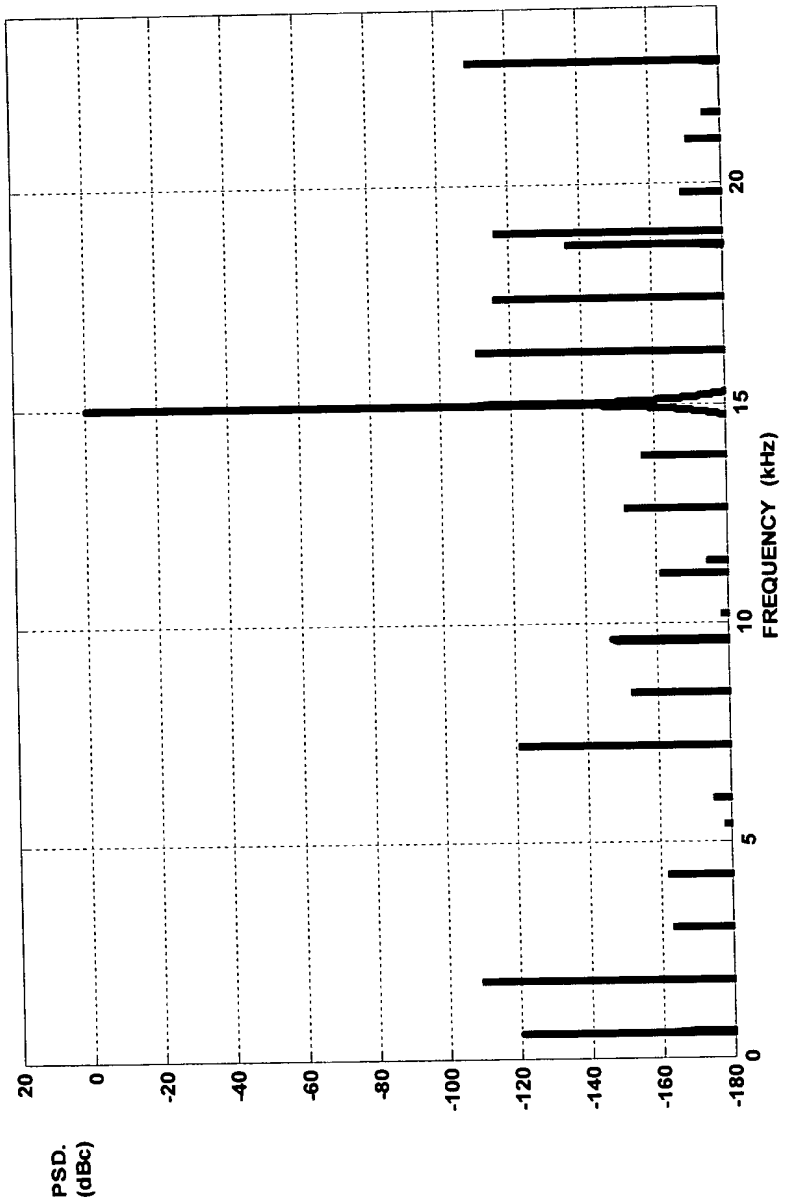


Figure 15: Typical in-band ripple of the interpolator magnitude response



16: Typical output power spectral density of the sampling rate converter

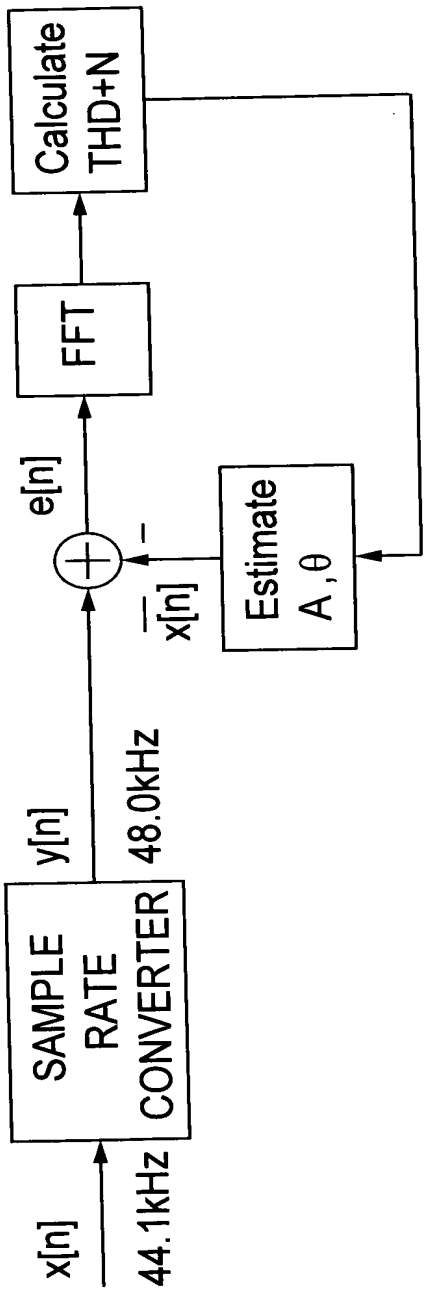


Figure 17: Scheme for calculating SNDR and SFDR via simulation

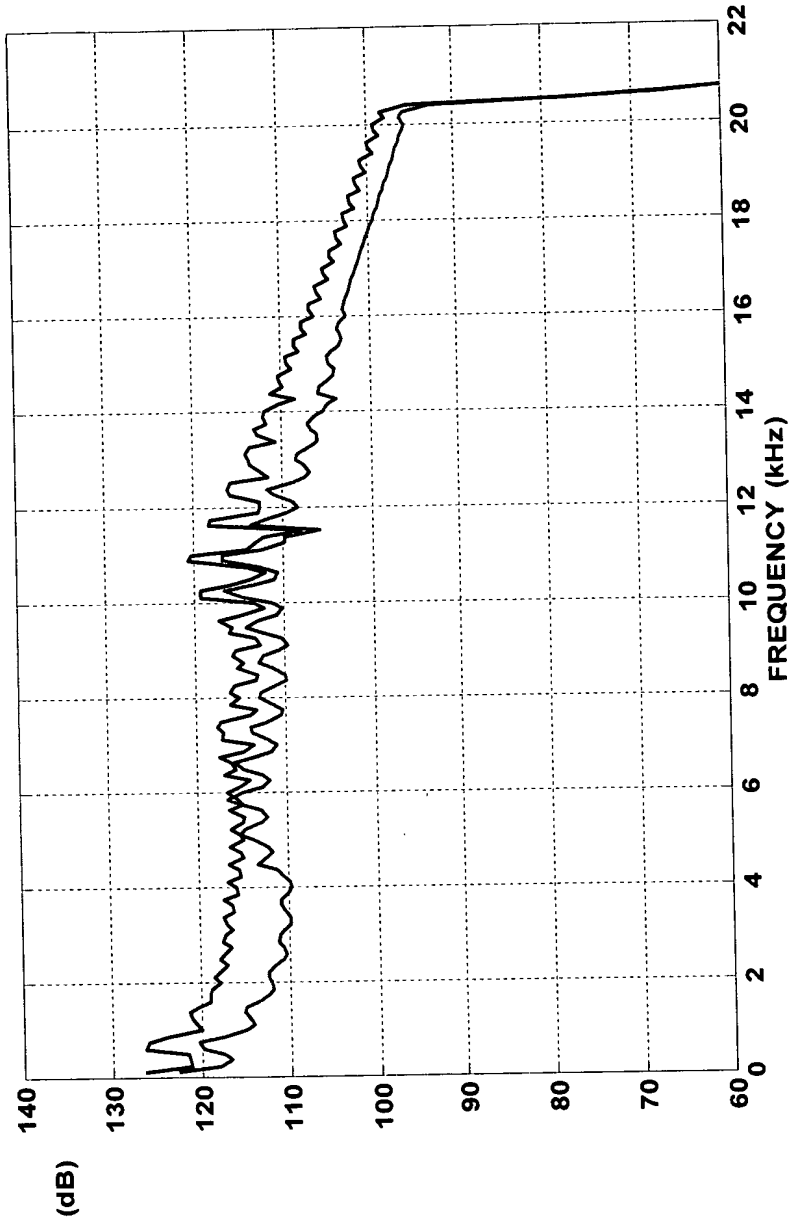


Figure 18: Simulated spurious-free dynamic range (SFDR) (blue) and signal-to-noise-and-distortion ratio (SNDR) (red) vs. frequency of the sampling rate converter output.

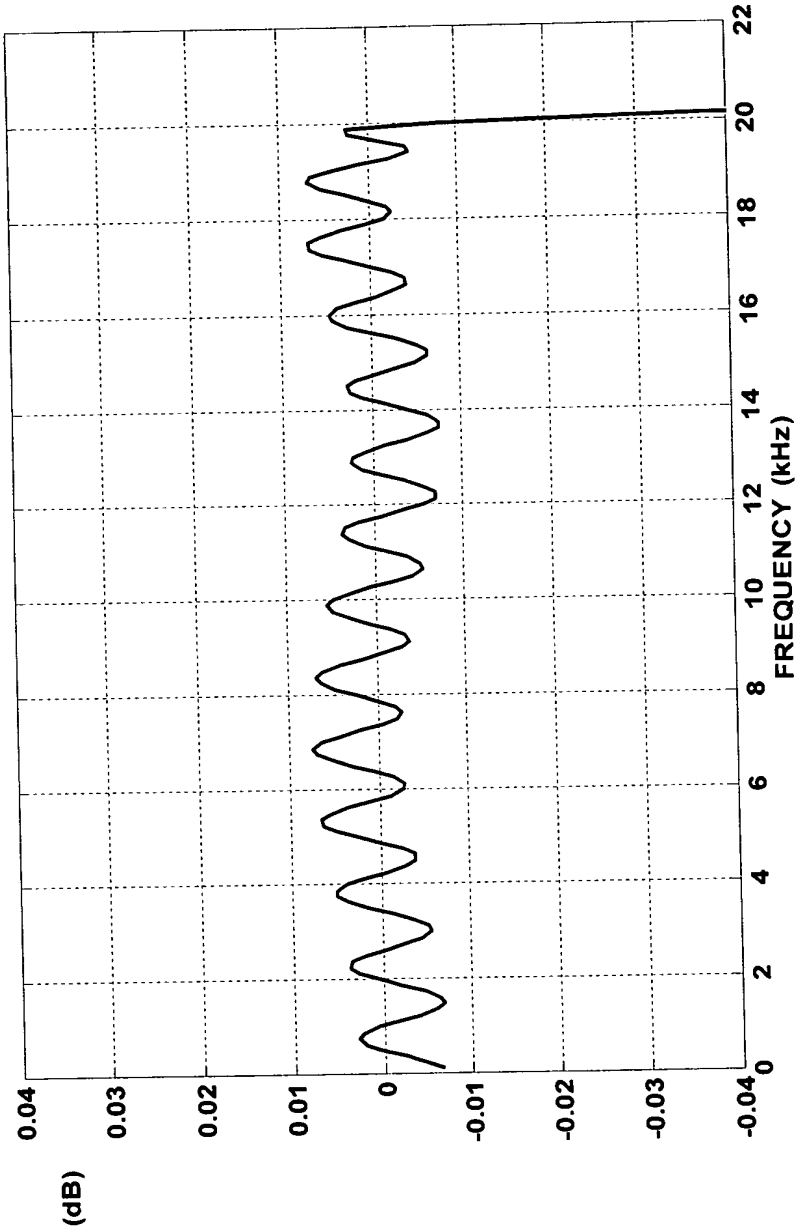


Figure 19: Simulated magnitude response of the sampling rate converter.